Amendment to the Claims

Kindly amend claims 1-12, and add new claims 13-18, as set forth below. In compliance with the Revised Amendment Format published in the Official Gazette on February 25, 2003, a complete listing of claims is provided herein. The changes in the amended claims are shown by strikethrough (for deleted matter) and underlining (for added matter).

1. (Currently Amended) A method of providing error detection and correction in an interface between two portions of a data processing system, the method comprising:

generating, in a first portion of the data processing system, parity bits corresponding to ~~substantially the entirety~~ a plurality of bits ~~contained in~~ of the interface;

transmitting across the interface the parity bits together with the ~~entirety~~ plurality of bits ~~contained in~~ of the interface;

testing, in a second portion of the data processing system, that the parity bits correspond to the plurality of bits for which parity was encoded; and

detecting and correcting, in [a] the second portion of the data processing system, one or more errors in the plurality of bits for which parity was encoded.

2. (Currently Amended) The method according to claim 1, wherein the interface is a ~~connector~~ non-integrated intermittent interconnection.

3. (Currently Amended) The method according to claim 1, wherein the ~~interface includes~~ plurality of bits for which parity was encoded include data, address and control signals.

4. (Currently Amended) The method according to claim 1, wherein an indication is provided to the data processing system of corrected errors.

5. (Currently Amended) The method according to claim 1, wherein an indication is provided to the data processing system of uncorrected errors.

6. (Currently Amended) The method according to claim 1, wherein single bit errors are detected and corrected.

7. (Currently Amended) A system for error detection and correction in an interface between two portions of a data processing system, the system comprising:

a parity generator, in a first portion of the data processing system, for generating parity bits corresponding to ~~substantially the entirety~~ a plurality of bits ~~contained in~~ of the interface;

~~an~~ the interface for transmitting the ~~data~~ plurality of bits and the parity bits;

a parity checker, in a second portion of the data processing system, for checking that the parity bits correspond to the plurality of bits for which parity was encoded; and

an error correction circuit, in [a] the second portion of the data processing system, for correcting one or more errors in the plurality of bits for which parity was encoded.

8. (Currently Amended) The system according to claim 7, wherein the interface is a ~~connector~~ non-integrated intermittent interconnection.

9. (Currently Amended) The system according to claim 7, wherein the ~~interface includes~~ plurality of bits for which parity was encoded include data, address and control signals.

10. (Currently Amended) The system according to claim 7, wherein an indication is provided to the data processing system of corrected errors.

11. (Currently Amended) The system according to claim 7, wherein an indication is provided to the data processing system of uncorrected errors.

12. (Currently Amended) The ~~method~~ system according to claim 7, wherein single bit errors are detected and corrected.

13. (New) The method of claim 1, wherein the first portion comprises a sending portion and the second portion comprises a receiving portion.

14. (New) The method of claim 1, wherein the detecting and correcting are performed transparently wherein a sender of the plurality of bits need not know of the one or more errors.

15. (New) The method of claim 1, wherein the detecting and correcting are performed asynchronously.

16. (New) The method of claim 1, wherein the correcting comprises reconstructing one or more bits of the plurality of bits using the transmitted bits of the interface.

17. (New) The method of claim 15, wherein the reconstructing uses the transmitted bits to reconstruct the one or more bits regardless of a nature of the error.

18. (New) The method of claim 1, wherein multiple bit errors are detected and corrected.